

ABSTRACT

In a semiconductor device of the present invention, a clock is not changed instantaneously but it is changed over maximum $N+1/M$ clocks (N : integer not less than 2) by shifting delay cells in a step by step manner to make the phase state of a previous reference signal and the phase state of a present reference signal coincide with each other, whereby the clock is synchronized with the reference signal with accuracy, and the duty of the output clock is kept constant. With this semiconductor device, it is possible to prevent the duty of the clock from being discontinuous when a signal whose reference signal does not coincide with the clock is inputted and reset is made to a rising edge of this reference signal.